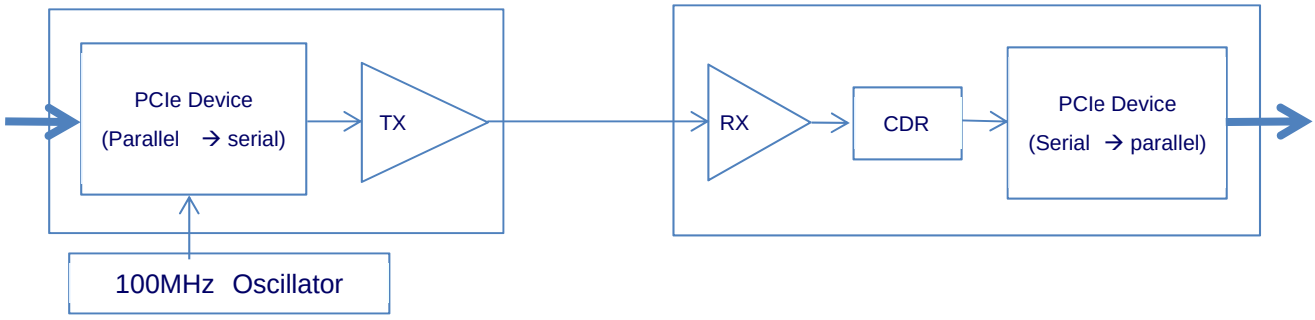
EPSON timing solution for Altera® FPGA
Stratix® V, Arria® V, Cyclone® V Transceiver PCI Express® Gen1, 2

PCI Express® (PCIe®) is a high-speed serial transmission widely adopted in PC, server, FA equipment's, measurement equipment's, broadcast products etc. FPGAs provide PCIe® transceivers for these applications.
Epson oscillators have been confirmed as reference clock functionality by actual evaluations.

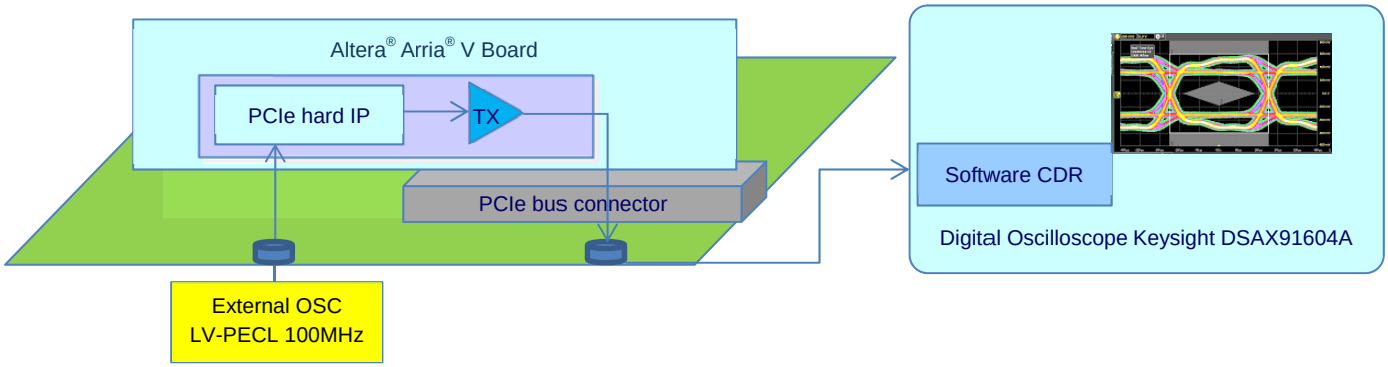
<Method of reference clock availability confirm >

1. Connect Epson oscillator to Altera Arria® V PCIe® board as reference clock.
2. Measure PCIe® TX output with oscilloscope.
3. Calculate BER with oscilloscope's Eye Diagram and RMS data.

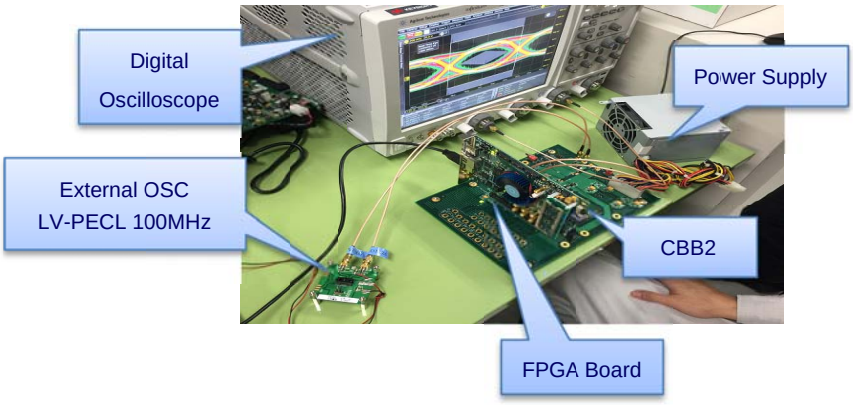
<Basic PCIe Transceiver diagram>



<Basic Measurement schematic>



<Measurement scene>



PCIe® TX oscillator measurement result, PCIe® Transmission performance

Evaluation result of 3 oscillators (XG-2102CA, SG7050EBN, Other). XG-2102CA has the best performance.

BER (bit error rate) Calculated by RMS jitter	Oscillator (100MHz Reference Clock)		
	Other oscillator	XG-2102CA	SG7050EBN
PCIe Gen.1 (2.5 Gbps)	1.2×10^{-20}	1.3×10^{-27}	**7.5×10^{-31} (Best)**
PCIe Gen.2 (5 Gbps)	7.9×10^{-08}	4.5×10^{-08}	**2.6×10^{-08} (Best)**

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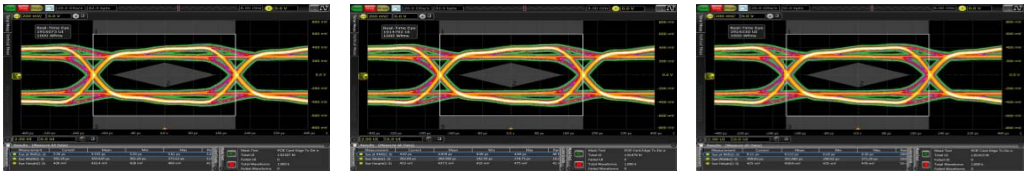
<PCIe® Gen.1 Data speed 2.5 Gbps>

RMS and Eye Pattern

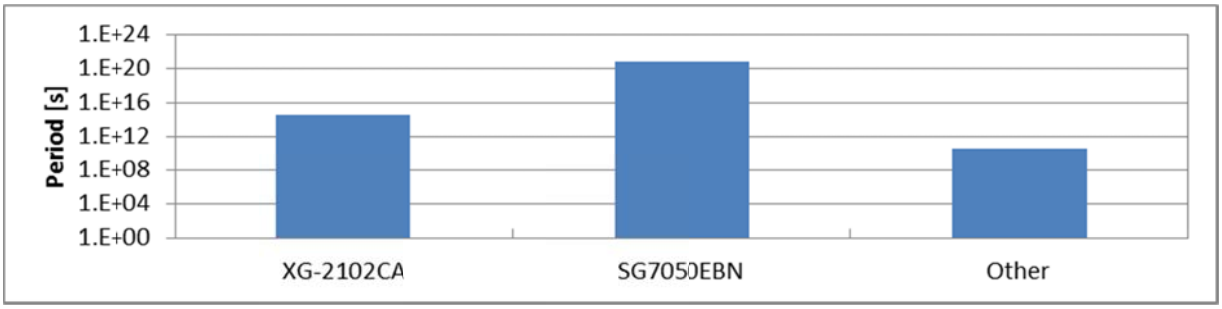
Eye Diagram Jitter RMS (Unit : ps)	Oscillator (100MHz reference Clock)		
	XG-2102CA	SG7050EBN	Other oscillator
(2nd PLL CDR)	5.56	4.92	6.11



BER (bit error rate) calculated with RMS.

BER (bit error rate) Capitulated by RMS jitter	Oscillator (100MHz reference Clock)		
	XG-2102CA	SG7050EBN	Other oscillator
(2nd PLL CDR)	1.3×10^{-27}	7.5×10^{-31}	1.2×10^{-20}

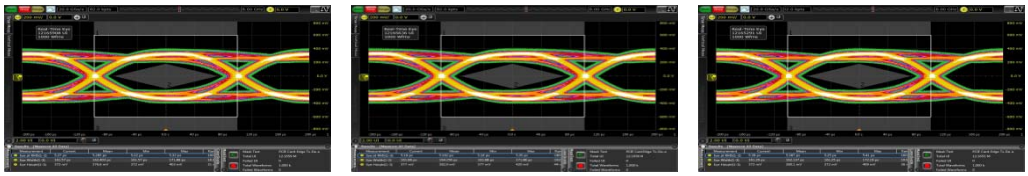
The timing period to the first error occasion. (Unit: sec).



<PCIe® Gen.2 Data speed 5 Gbps>

RMS and Eye Pattern

Eye Diagram Jitter RMS (Unit : ps)	Oscillator (100MHz reference Clock)		
	XG-2102CA	SG7050EBN	Other oscillator
(2nd PLL CDR)	5.29	5.19	5.39



BER (bit error rate) calculated with RMS.

BER (bit error rate) Capitulated by RMS jitter	Oscillator (100MHz reference Clock)		
	XG-2102CA	SG7050EBN	Other oscillator
(2nd PLL CDR)	4.5×10^{-08}	2.6×10^{-08}	7.9×10^{-08}

The timing period to the first error occasion. (Unit: sec).