

Methods for Achieving High-Frequency Output (Part 1: PLL Circuits)

PLL Circuit Overview and Epson Product Lineup

Preface

Data transmission speeds and volume continue to increase to support unabated growth in traffic flowing over the Internet backbone largely due to the spread of movie and other content delivery services. The need for high-speed communications infrastructure is driving strong demand for high-frequency reference signal sources that provide stable output signals. Generally speaking, for a MHz range AT-cut crystal unit to oscillate at high frequencies, the thickness of the crystal chip has to be reduced (since the thickness determines the frequency at which an AT-cut crystal unit oscillates) but there are limits in respect to processing methods, mechanical strength, and ease of oscillation. Although it depends on processing accuracy, 60 MHz is as limitation for the fundamental frequency of AT-cut crystal. For this reason, Epson positioned over 60 MHz as the high-frequency range. Producing such a stable high-frequency reference signal is not so simple, but Epson has four methods (technologies) for achieving high-frequency oscillation. In the first method, an AT-cut crystal unit that produces a relatively manageable oscillation frequency on the order of 20 MHz is combined with a frequency multiplier circuit or phase-locked loop (PLL) circuit to produce a stable, high-frequency reference signal. The second method for producing a high-frequency, stable reference signal is to use a surface acoustic wave (SAW) resonator, which directly oscillates at a high frequency fundamental. The third method is to use an inverted-mesa type AT-cut crystal unit, wherein only the vibrating portions of the crystal are thinned using Epson's QMEMS process technology. The fourth method is to use a vibration mode (overtone) that vibrates at a high order of the AT-cut crystal unit. These Technical Notes provide a summary explanation of the first method, the method using frequency multiplier circuits (here, multiplier circuit refers to analog multipliers that extract harmonic components) and PLL circuits.

1. Frequency multiplier circuits provide high-frequency output to nth degree

A frequency multiplier circuit is a circuit that converts the electric signal of a certain frequency into a high frequency increased to the nth degree. With output signals from typical oscillation circuits, the formation of a certain level of T_r , T_f , V_{oh} , and V_{ol} creates a waveform containing harmonic components. The frequency multiplier circuit intentionally creates a signal that emphasizes the nth component from these harmonics, after which a filter is used to extract the nth component. Using the harmonic components achieves an output frequency with less jitter than a PLL. However, when using filters that only extract the nth harmonic, a narrow-bandwidth/ band-pass filter (BPF) must be used to dampen low ($n/2$ and lower) signal components (sub harmonics) and limit jitter. Also, care must be taken when selecting a crystal unit and when designing the oscillation circuit so that the source signal does not generate spurious signals near the nth harmonic.

As such, the technology used in products for gaining high frequency often involves PLL circuits. The next chapter provides an explanation of PLL circuits.

2. PLL circuits

The following is an explanation of PLL circuits, another basic technology for producing stable, high-frequency signals. Semiconductor technology for wireless communications has advanced dramatically with the dissemination of devices that include wireless communications components. Among such technologies, innovation in PLL circuit technology has particularly been astounding.

A PLL circuit generates an output signal that is synchronized with the input reference signal. With the basic structure that comprises of a phase comparator, loop filter, and voltage-controlled oscillator (VCO), a PLL circuit is capable of producing a signal that is accurately synchronized with the input signal. Unlike frequency multiplier circuits, the source signal is not used for output. PLL circuits use

the VCO to generate a synchronized signal at a frequency that differs from the source signal.

By inserting a frequency demultiplier between the PLL circuit VCO output and the phase comparator input, synchronizing the input signal and divided signal, the VCO output is controlled to a frequency obtained by multiplying the input frequency by the demultiplication ratio. To attain this VCO output to an accuracy equivalent to a crystal oscillator, it is necessary to change the demultiplication ratio while using a crystal oscillator or similar component that can generate stable input signals. This is the principle behind the frequency synthesizer.

Applying this principle, the MHz band output of an AT-cut crystal unit is input to a PLL circuit to create a signal that generates a GHz band carrier wave for use in wireless communications.

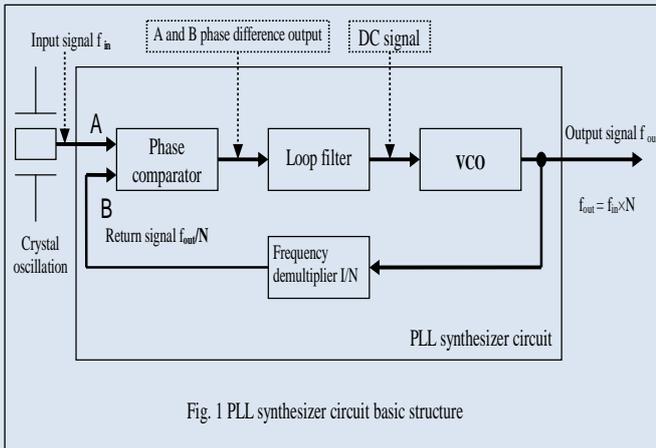


Fig. 1 PLL synthesizer circuit basic structure

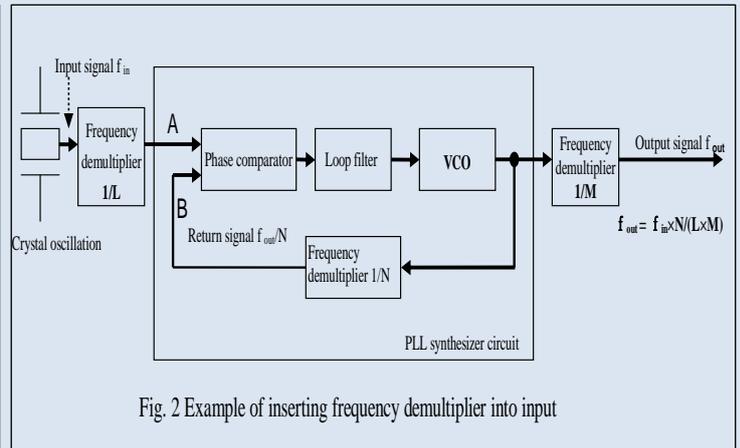


Fig. 2 Example of inserting frequency demultiplier into input

The key to using a PLL circuit to generate a high frequency that is many times greater than the input frequency lies in how the frequency demultiplier is used. The method for achieving nth degree output of the input frequency is the circuit configuration indicated in Figure 1. Also, as shown in Figure 2, inserting a demultiplying circuit before and after the PLL circuit I/O allows for precise adjustments to the output frequency.

A typical means for increasing frequency setting resolution in a PLL circuit involves introducing a frequency demultiplier directly after the crystal oscillation source. However, using a higher divided frequency to increase frequency setting resolution causes a lower phase comparison frequency, which results in a decline in PLL responsiveness and loop gain. These in turn negatively impact on output waveform jitter and phase noise characteristics. A method for resolving this problem is to use a fractional PLL, for example.

3. Characteristics of Integer PLL and Fractional PLL

PLL circuits are largely divided into two types: integer and fractional. Both types use an oscillating source to output a high-frequency signal. Below is an explanation of major characteristics.

As the name suggests, an integer PLL is capable of creating output frequencies that are integral multiples of the input frequency. For example, if you want to output a 100MHz signal from a 1MHz source, the demultiplier counter setting is 100.

Conversely, a fractional PLL is capable of creating output frequencies that are fractional multiples of the input frequency. The benefit of this circuit is that it allows you to select any frequency (enables you to obtain precise frequency setting resolution).

A fractional PLL allows for precise frequency resolution setting, the initial frequency deviation can precisely be controlled with these properties.

However, the downside is that the circuit design is complicated and the size of an IC becomes larger when compared to integer PLLs, meaning that a particular spurious tends to occur. As a result, it is generally thought that fractional PLLs generate more phase noise than integer PLLs. However, with recent technological advancements, efforts are progressing to reduce the occurrence of spurious which thus far has been a weakness of using fractional PLLs.

4. Epson product lineup and product features

Above, we examined methods for employing PLL circuits as a way to achieve high-frequency output. The greatest characteristic of these methods is the ability to create a desired frequency at will. In other words, these methods provide necessary frequencies, including high frequencies, when you need them.

Epson's SG-8000 series, which utilizes the integer PLL circuit technology introduced above, offers a diverse product lineup featuring various shapes and sizes (Table 1). We also offer a ROM writer (SG-Writer II) as a programming tool that allows customers to write frequency commands to the SG-8000 series (Table 2).

The SG-8000 series uses an AT-cut crystal unit. The cubic curve temperature properties of the AT-cut crystal unit, which maintains given temperature stability, enables us to offer products with smooth frequency characteristics (without frequency jumps) that do not require temperature-based compensations in a wide range. (Oscillators with first-order linearity of significant temperature properties such as Si-MEMS oscillators require circuit compensations to maintain stability at a given temperature and can result in an occurrence of frequency jumps.)

We look forward to helping our customers experience the highly accurate characteristics of these crystal units combined with the convenience of discretionary frequency settings achieved through the PLL circuit technology.

Lastly, provided below are some points of caution concerning "multiplying" and "PLL" as methods used to achieve high-frequency output.

Multiplying: Be careful of subharmonic components being generated in the circuits, and jitter caused by components below $n/2$.

PLL: Note the loop bandwidth and be careful of jitter amplification and tracking when being connected to the subsequent PLL.

Table 1: Programmable crystal oscillator product lineup

Product	Output	Type	Frequency					
			1 Hz	1 MHz	50 MHz	100 MHz	500 MHz	800 MHz
SG-8003 series (1.8/2.5/3.3 V)	CMOS	CG, CE, LB, JF, CA	1.0 MHz				166 MHz	
SG-8002 series (3.3 / 5.0 V)		CE, LB, JF, CA, JC, JA, DC, DB	1.0 MHz				125 MHz	

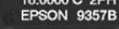
Type	CG	CE	LB	JF	CA	JC	JA	DC	DB
External dimensions (mm)	2.5×2.0×0.8 (t: Max.)	3.2×2.5×1.05 (t: Typ.)	5.0×3.2×1.2 (t: Max.)	7.1×5.1×1.5 (t: Max.)	7.0×5.0×1.4 (t: Typ.)	10.5×5.8×2.7 (t: Max.)	14.0×9.8×4.7 (t: Max.)	DIP half size	DIP full size
									

Table 2: SG-8000 Series Programming Tool

	SG-Writer II
Connector terminal	USB2.0 (Min-b)
Compatible OS	Windows 7 (32 bit, 64 bit) Windows Vista (32 bit) Windows XP (32 bit)
Socket	GS-8002, SG-8003 Both sockets are writable
Software	SG-Writer II software