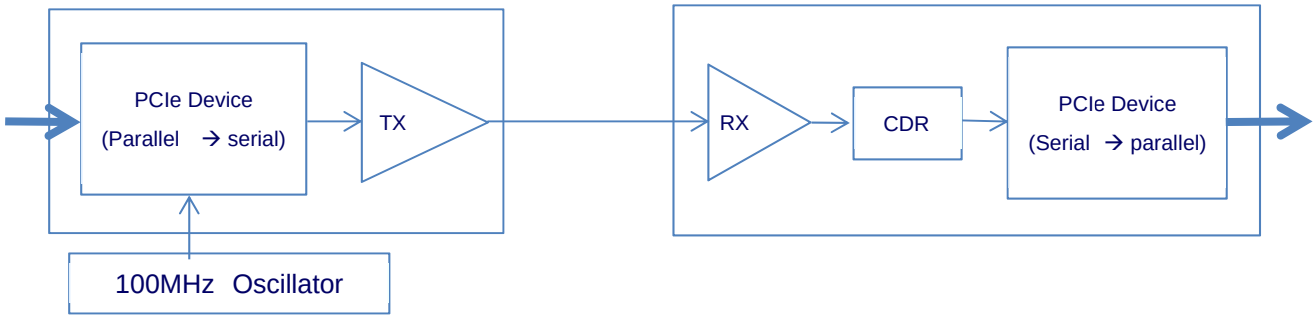
EPSON timing solution for Xilinx® FPGA
Virtex®, Kintex®, Artix®-7 series Transceiver PCI Express® Gen1, 2

PCI Express® (PCIe®) is a high-speed serial transmission widely adopted in PC, server, FA equipment's, measurement equipment's, broadcast products etc. FPGAs provide PCIe® transceivers for these applications. Epson oscillators have been confirmed as reference clock functionality by actual evaluations.

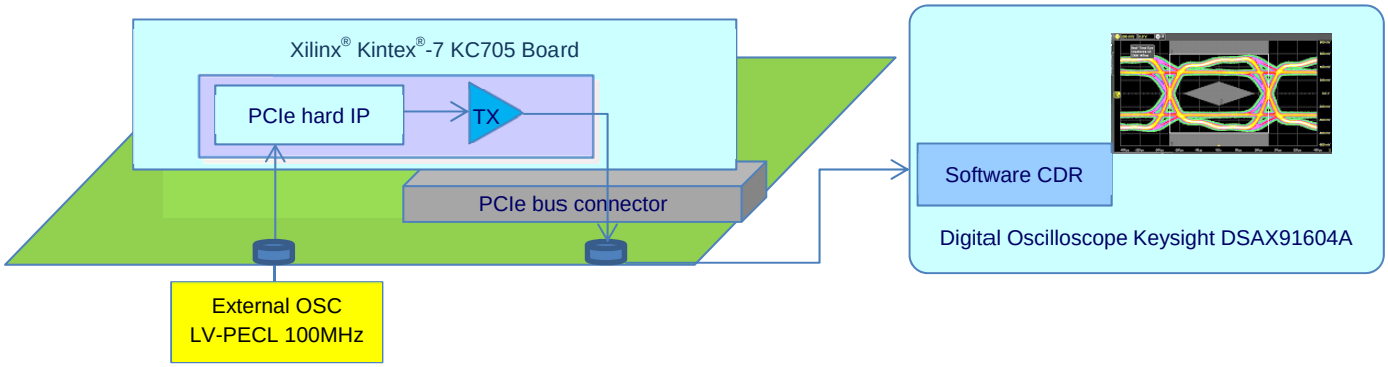
< Method of Reference clock availability confirm >

1. Connect Epson oscillator to Xilinx® Kintex®-7 PCIe® board as reference clock.
2. Measure PCIe® TX output with oscilloscope.
3. Calculate BER with oscilloscope's Eye Diagram and RMS data.

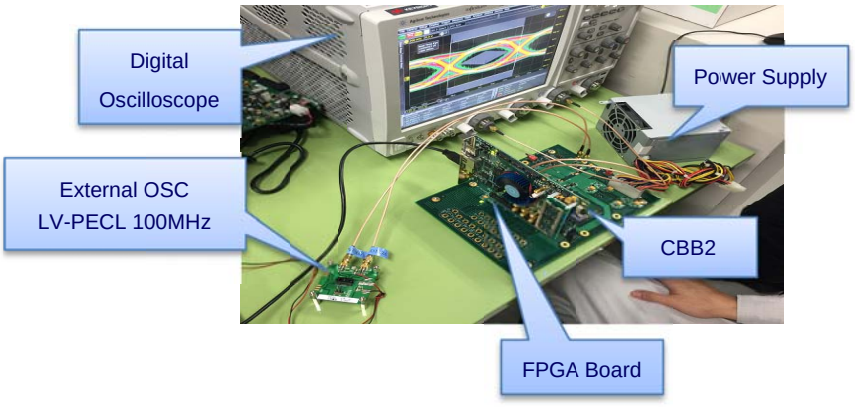
<Basic PCIe Transceiver diagram>



<Basic Measurement schematic>



<Measurement scene>



PCIe® TX oscillator measurement result, PCIe® Transmission performance

Evaluation result 3 oscillators（XG-2102CA, SG7050EBN, Other）. XG-2102CA has the best performance.

BER (bit error rate) Calculated by RMS jitter	Oscillator (100MHz Reference Clock)		
	Other oscillator	XG-2102CA	SG7050EBN
PCIe Gen.1 (2.5 Gbps)	**1.3 x 10 $^{-47}$ (Best)**	2.3 x 10 $^{-36}$	4.0 x 10 $^{-12}$
PCIe Gen.2 (5 Gbps)	**5.6 x 10 $^{-17}$ (Best)**	1.4 x 10 $^{-16}$	9.9 x 10 $^{-16}$

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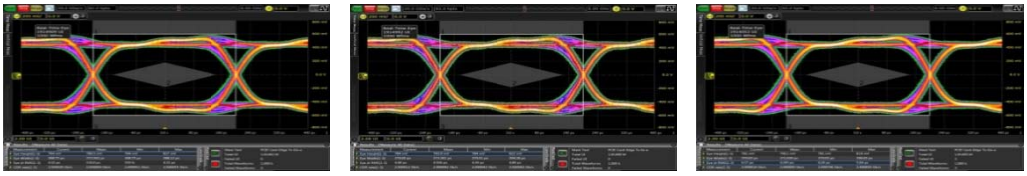
<PCIe® Gen.1 Data speed 2.5 Gbps>

RMS and Eye Pattern

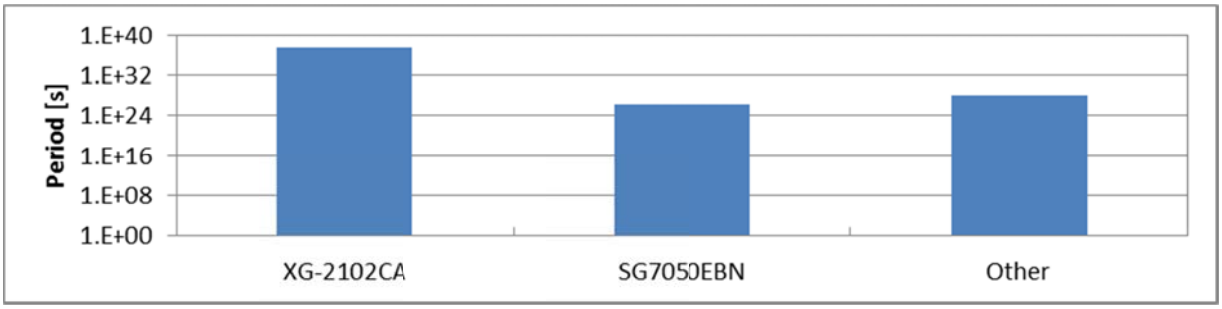
Eye Diagram Jitter RMS (Unit : ps)	Oscillator (100MHz reference Clock)		
	XG-2102CA	SG7050EBN	Other oscillator
(2nd PLL CDR)	3.91	4.51	4.40



BER (bit error rate) calculated with RMS.

BER (bit error rate) Capitulated by RMS jitter	Oscillator (100MHz reference Clock)		
	XG-2102CA	SG7050EBN	Other oscillator
(2nd PLL CDR)	1.3×10^{-47}	2.3×10^{-36}	4.0×10^{-38}

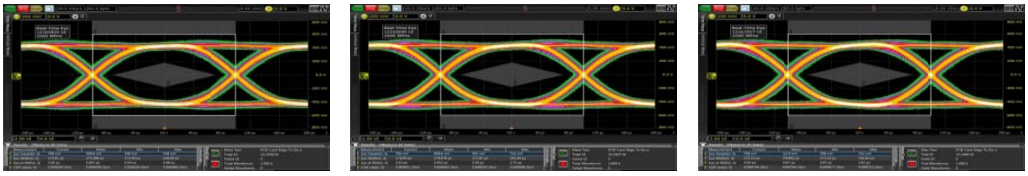
The timing period to the first error occasion. (Unit: sec).



<PCIe® Gen.2 Data speed 5 Gbps>

RMS and Eye Pattern

Eye Diagram Jitter RMS (Unit : ps)	Oscillator (100MHz reference Clock)		
	XG-2102CA	SG7050EBN	Other oscillator
(2nd PLL CDR)	3.41	3.45	3.56



BER (bit error rate) calculated with RMS.

BER (bit error rate) Capitulated by RMS jitter	Oscillator (100MHz reference Clock)		
	XG-2102CA	SG7050EBN	Other oscillator
(2nd PLL CDR)	5.6×10^{-17}	1.4×10^{-16}	9.9×10^{-16}

The timing period to the first error occasion. (Unit: sec).