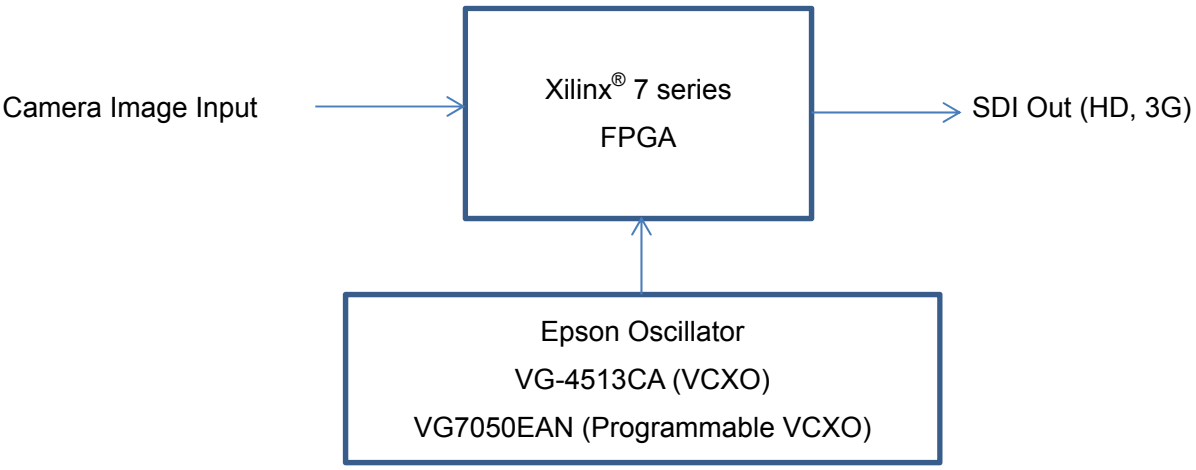
EPSON timing solution for Xilinx® FPGAs

EPSON は、ネットワーク機器をはじめ医療機器、計測器、放送機器等に多く用いられる FPGA に向けたリファレンスクロックを各種用意しております。

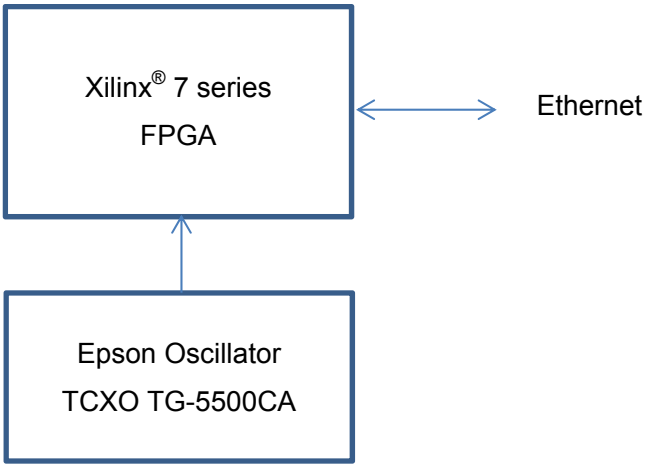
高速シリアル伝送用トランシーバ用	:	低ジッタ SPXO
放送、映像機器用 SDI 信号用	:	VCXO，プログラマブル VCXO
時刻動機 IEEE1588,SyncEther 用	:	高安定 TXCO

＜高速シリアル通信＞

＜放送、映像伝送＞



＜時刻同期システム＞



EPSON timing solution
For Xilinx® FPGA Transceiver

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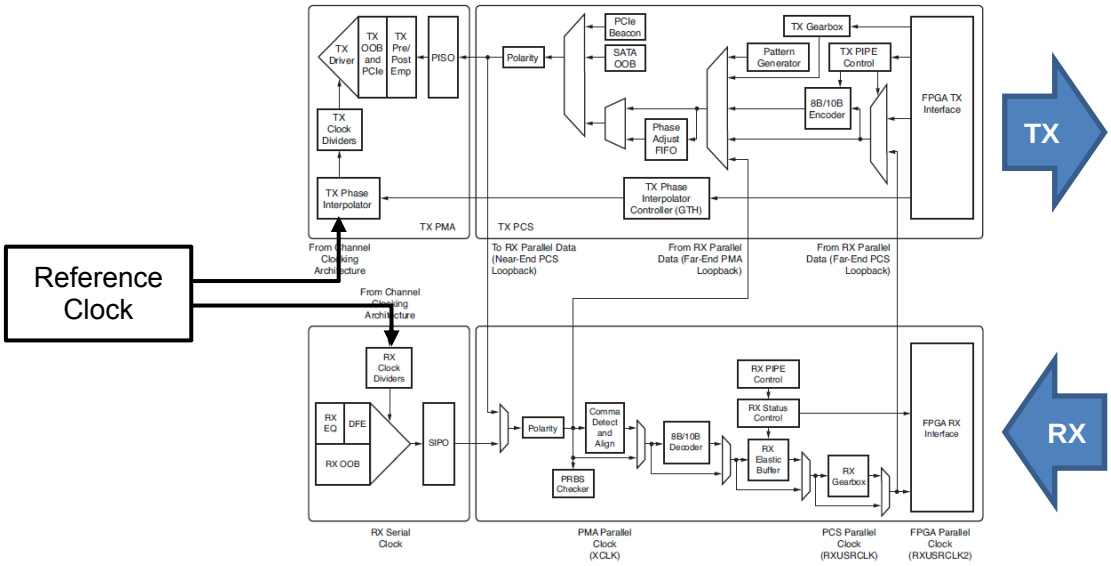
Xilinx® 7 series FPGA transceiver block diagram



Recommended Products Line-up

Product name	Image Size [mm]	Frequency Range	Supply voltage	Output	Phase Jitter (12 k to 20 MHz)	Features
XG-2102CA (SPXO)	 7×5×1.2t	100 MHz to 700 MHz	3.3 V	LVDS LV-PECL	0.23 ps Max. (f<150 MHz) 0.22 ps Max. (150 M≤f<200 MHz) (Note1)	SAW based low jitter crystal oscillator
MG7050EAN (SPXO)	 7×5×1.6t			LV-PECL (2 or 4 outputs)	0.17 ps Max. (f=100 MHz) 0.15 ps Max. (f=156.25 MHz) (Note2)	
SG7050EBN (SPXO)	 7×5×1.5t	100 MHz to 175 MHz	3.3 V	LV-PECL	0.14 ps Max. (f=100 MHz) 0.1 ps Max. (f=156.25 MHz) (Note3)	Fundamental oscillation, low phase noise crystal oscillator
VG-4513CA (VCXO)	 7×5×1.6t	100 MHz to 500 MHz	3.3 V	LV-PECL	0.24 ps Typ. (f=122.88 MHz) (Note4)	High frequency fundamental oscillation by HFF, low noise and low jitter VCXO
VG7050EAN (VCXO)	 7×5×1.5t	50 MHz to 800 MHz	3.3 V	LV-PECL	0.3 ps Typ. (f=122.88 MHz) 0.26 ps Typ. (f=153.6 MHz) (Note5)	Low power and low noise Programmable VCXO by Fractional-N PLL

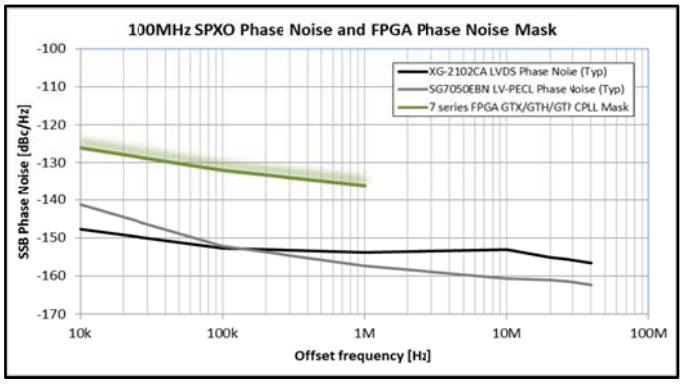
Note1 detail specification http://www5.epsondevice.com/ja/products/spxo_low_jitter/xg2102ca.html
Note2 detail specification http://www5.epsondevice.com/ja/products/spxo_low_jitter/mg7050ean.html
Note3 detail specification http://www5.epsondevice.com/ja/products/spxo_low_jitter/sg7050ebn.html
Note4 detail specification http://www5.epsondevice.com/ja/products/vcxo_low_phase_noise/vg4513ca.html
Note5 detail specification http://www5.epsondevice.com/ja/products/vcxo_low_phase_noise/vg7050ean.html

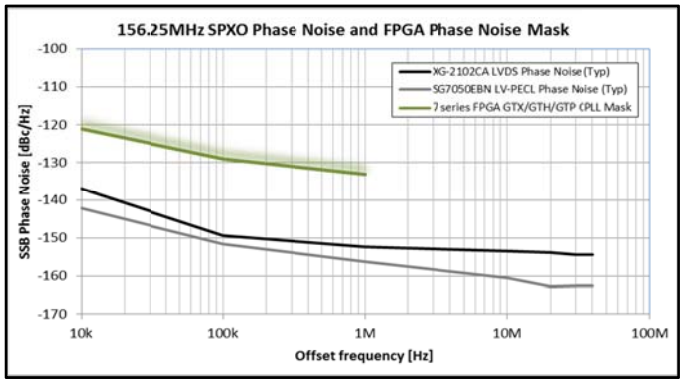
Jitter Performance for Xilinx® 7 series FPGA

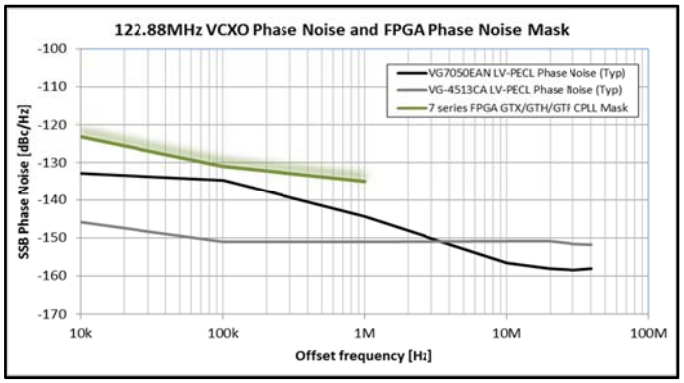
EPSON clocks meet Xilinx® FPGA transceiver reference clock jitter requirement.

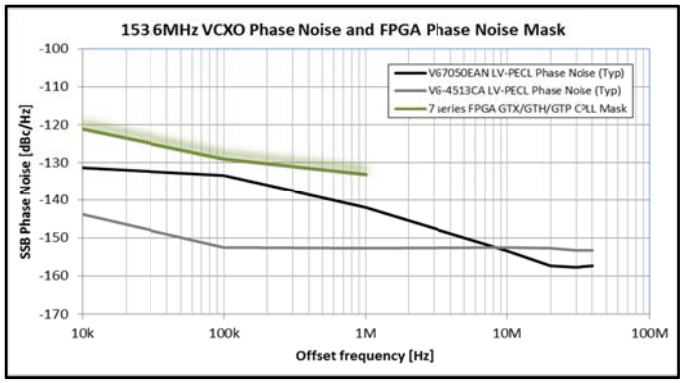
		GTX / GTH (QPLL)			GTX / GTH / GTP (CPLL)		
		At 10 kHz	At 100 kHz	At 1 MHz	At 10 kHz	At 100 kHz	At 1 MHz
100 MHz SPXO	Requirement	-126 dBc/Hz	-130 dBc/Hz	-134 dBc/Hz	-126 dBc/Hz	-132 dBc/Hz	-136 dBc/Hz
	XG-2102CA,MG7050EAN	-148 dBc/Hz	-153 dBc/Hz	-154 dBc/Hz	-148 dBc/Hz	-153 dBc/Hz	-154 dBc/Hz
	SG7050EBN	-141 dBc/Hz	-152 dBc/Hz	-157 dBc/Hz	-141 dBc/Hz	-152 dBc/Hz	-157 dBc/Hz
156.25 MHz SPXO	Requirement	-122 dBc/Hz	-127 dBc/Hz	-132 dBc/Hz	-121 dBc/Hz	-129 dBc/Hz	-133 dBc/Hz
	XG-2102CA,MG7050EAN	-137 dBc/Hz	-149 dBc/Hz	-152 dBc/Hz	-137 dBc/Hz	-149 dBc/Hz	-152 dBc/Hz
	SG7050EBN	-142 dBc/Hz	-152 dBc/Hz	-156 dBc/Hz	-119 dBc/Hz	-126 dBc/Hz	-132 dBc/Hz
122.88 MHz VCXO	Requirement	-123 dBc/Hz	-129 dBc/Hz	-133 dBc/Hz	-123 dBc/Hz	-131 dBc/Hz	-135 dBc/Hz
	VG-4513CA	-146 dBc/Hz	-151 dBc/Hz	-151 dBc/Hz	-146 dBc/Hz	-151 dBc/Hz	-151 dBc/Hz
	VG7050EAN	-133 dBc/Hz	-135 dBc/Hz	-144 dBc/Hz	-133 dBc/Hz	-135 dBc/Hz	-144 dBc/Hz
153.6 MHz VCXO	Requirement	-122 dBc/Hz	-127 dBc/Hz	-132 dBc/Hz	-121 dBc/Hz	-129 dBc/Hz	-133 dBc/Hz
	VG-4513CA	-144 dBc/Hz	-153 dBc/Hz	-153 dBc/Hz	-144 dBc/Hz	-153 dBc/Hz	-153 dBc/Hz
	VG7050EAN	-131 dBc/Hz	-134 dBc/Hz	-142 dBc/Hz	-131 dBc/Hz	-134 dBc/Hz	-142 dBc/Hz

◆ Phase Noise plot and GTX/GTH/GTP(CPLL) Mask



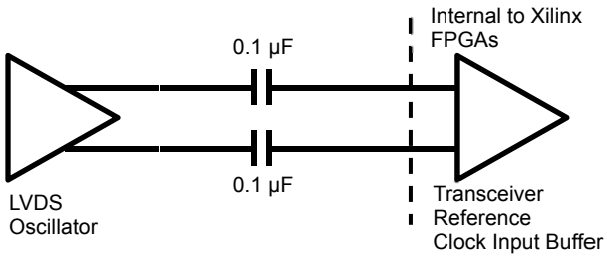




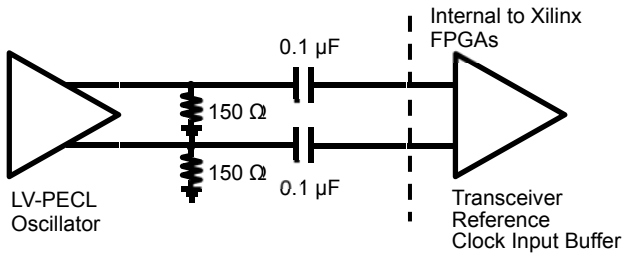


Recommended Reference Clock Interface

◆ LVDS LV-PECL



◆ LV-PECL

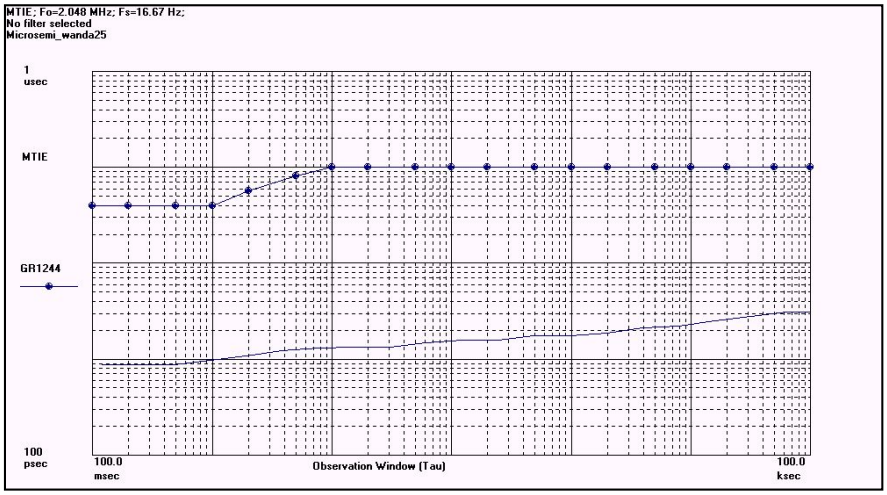


EPSON timing solution
For Xilinx® FPGA Timing Synchronization

Recommended Products Line-up

Product name	Image Size [mm]	Frequency Range	Supply voltage	Output	Frequency Stability (-40 to +85 degC)	Features
TG-5500CA (TCXO)	 7×5×1.2t	10 MHz to 50 MHz	3.3 V	CMOS/ Clipped Sine	+/-280 ppb	Stratum3 compatible
TG5032CBN TG5032SBN (TCXO)	 5×3.2×1.45t	10 MHz to 40 MHz	3.3 V	CMOS/ Clipped Sine	+/-280 ppb	Stratum3 compatible

TG-5500CA 24.576 MHz　MTIE data　(0.1Hz filter)



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